MSAS-72

MT9042A and MT9042B Differences

Application Sheet

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Introduction

This application sheet compares the MT9042B functionality with that of the MT9042A. The initial alpha trials of the MT9042A indicated that some enhancements were required to gain wider customer acceptance of the product. These enhancements will help meet and exceed standards, and reduce hardware and software overhead.

The MT9042B is a pin to pin compatible enhanced version of the MT9042A. Every effort was made to design the MT9042B such that backwards compatibility with the MT9042A was maintained. Most systems currently using the MT9042A will be able to accept the MT9042B with little or no modifications to their existing hardware and software. However, systems which require the MT9042A's extra wide capture range and very fast lock time may find the MT9042B unsuitable.

Table 1 below illustrates the functional differences between the two devices. Some additional details are provided in the following section, but for full details on the MT9042B functionality, refer to the MT9042B data sheet.

Item	Description	MT9042A	MT9042B
1	Reference switching.	Cycle slips may occur in the presence of jitter.	No cycle slips.
2	Holdover to Normal Mode changes.	Cycle slip may occur.	No cycle slips.
3	Capture range, lock range, output frequency range.	12,600ppm	230ppm
4	Phase change slope.	Function of input phase step.	Maximum of 5ns/125µs (53ns/ 1.326ms)
5	Phase continuity at the instance of reference and Mode switches.	Not maintained in all events.	Maintained in all events.
6	MTIE with bad signal.	1us maximum may not be always met.	1µs maximum always met.
7	Holdover Mode accuracy.	0.48ppm	0.05ppm
8	MTIE with Holdover to Normal Mode changes.	1µs maximum may not be always met.	1us maximum always met.
9	Holdover memory.	None	Between 30ms and 60ms.
10	GTi pin	Controls Mode changes.	Controls Mode changes and TIE corrector circuit.
11	GTo pin	Function of Control, LOS1 and GTi.	Function of LOS1.
12	$\overline{RST}$ pin	TTL type input. All outputs may be at logic high or logic low or active when $\overline{RST}$ at logic low.	Schmitt type input. All outputs fixed at logic high when $\overline{RST}$ at logic low.
13	$\overline{TRST}$	Phase shift to realignment is not always in the shortest direction.	Phase shift to realignment is always in the shortest direction.

Item	Description	MT9042A	MT9042B
14	Manual Control Mode changes.	Occur on falling edge of reference input.	Occur on rising edge of F8o.
15	Automatic Control Mode changes.	Occur on falling edge of reference input.	Occur on rising edge of F8o.
16	Pin 8. FP8-GCI frame pulse.	122ns wide positive frame pulse with falling edge aligned with the center or $\overline{F0o}$.	$\overline{F16o}$. 61ns wide negative frame pulse with center aligned with the center or $\overline{F0o}$.
17	Input to output phase alignment after a reset ($\overline{TRST}$ or $\overline{RST}$).	A function of the reference input and master clock frequency.	Always aligned. Independent of the reference input and master clock frequency.
18	Lock time	3s maximum	23s maximum
19	Loop filter	2.5Hz for E1 and 1.9Hz for T1	1.9Hz for both E1 and T1.
20	Jitter tolerance	Exceeds requirements by over 100%.	Exceeds requirements by about 30%.
21	Auto-Holdover State	None	When the frequency of the incoming signal is lost or outside of a pre-determined range, the device automatically enters Holdover Mode.

Table 1 - Functional Differences between the MT9042A and MT9042B

Functional Differences Details

Phase Change Slope (Item 4)

Depending on the reference input degradation (such as a complete loss of signal for 1ms), the MT9042A phase slope could exceed the AT&T TR62411 phase slope requirement of 81ns/1.326ms. In order to guarantee phase change slope compliance with all reference input degradations, a limiter (53ns/ 1.326ms) on the MT9042B was added.

This reduced phase slope also provides additional time (i.e., 10ms) for hardware to provide a loss of signal indication, and software to initiate a reference switch before the Maximum Time Interval Error (MTIE) is exceeded.

Lock Time (Item 18)

A reduction in phase change slope results in an increase in lock time. For identical frequencies 180˚ apart, the MT9042B lock time is about 1.5s. For frequencies at the end of the PLL range, lock time is about 30s. The MT9042A has a worst case lock time of about 3s.

Capture Range (Item 3)

In order to keep the lock time as small as possible and maintain the reduced phase change slope, the capture range for the MT9042B was reduced to 230ppm. Since the large capture range of the MT9042A (12,600ppm) was found to be unnecessary in all applications reviewed, impact of this change was deemed negligible.

Loop Filter (Item 19)

The reduction in cutoff frequency from 2.5Hz to 1.9 Hz ensures that the ETS 300-011 5.4.3.2 multiple user-network specification is met with sufficient margin. The 5Hz jitter at the output through a 40Hz to 100kHz bandpass filter is reduced in the MT9042B from about 0.12UIpp to 0.10UIpp, where the specification maximum is 0.11UIpp.